REMARKS

Claims 1-24 are pending and under consideration. In the non-final Office Action of December 18, 2006, the Examiner made the following disposition:

A.) Objected to the drawings.

B.) Rejected claims 10-13 under 35 U.S.C. §103(a) as being unpatentable over *Uya, et al.* in view of *Early.*

C.) Allowed claims 1-9 and 14-24.

Applicants address the Examiners disposition below.

A.) Objection to the drawings:

Applicants respectfully disagree with the objection.

The Examiner argues that the drawings must show additional drawing elements for "the image pickup device where electrons are accumulated with a negative gate voltage and the image pickup device where holes are accumulated with a positive gate voltage." *Office Action of 12/18/06*, page 2.

Applicants respectfully submit that additional drawing elements are not necessary for understanding this claimed subject matter. 35 U.S.C. 113; *See, also,* MPEP 608.02. Figures 5-8 and the related text in the specification (*see, e.g.,* page 28, line 15-29, line 2) clearly describe an image pickup device where electrons are accumulated with a negative gate voltage.

The specification at page 29, line 22-page 30, line 11, goes on to clearly describe how the image pickup device of Figures 5-8 is configured such that holes are accumulated with a positive gate voltage:

> In the above embodiments, the present invention is applied to an MOS type solid-state image pickup device in which signal charges are electrons, however, the present invention may be applied to an MOS type solid-state image pickup device in which signal charges are holes. In this case, the transfer transistor comprises a p-channel MOS transistor having the opposite conduction type to that described above. Accordingly, when charges are accumulated in the photodiode, a positive voltage, that is, a positive voltage which is increased to a value higher than the power source voltage is applied as the gate voltage of the p-channel transfer transistor. Further, the construction of the pixels in Figs. 5 to 8 is modified so that the conduction types of each substrate and each semiconductor region are inverted. The overflow path may be formed in the same manner.

As these two claimed embodiments are clearly described in the existing drawings and specification text, Applicants submit that additional drawing elements do not need to be shown for better understanding of the claims.

Applicants respectfully submit the objection has been overcome and request that it be withdrawn.

B.) Rejection of claims 10-13 under 35 U.S.C. §103(a) as being unpatentable over *Uya, et al.* in view of *Early*:

Claims 10-13 have been canceled.

C.) Allowance of claims 1-9 and 14-24:

Applicants respectfully acknowledge the Examiner's finding of allowable subject matter in claims 1-9 and 14-24.

CONCLUSION

It is submitted that claims 1-9 and 14-24 are patentable and that the application is in condition for allowance. Notice to that effect is requested.

Respectfully submitted,

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